

INFORMATION DISCLOSURE CITATION PTO-1449				<i>CS/10/2004</i>		
Sheet	1	of	1	Complete If Known		
				Application Number	To-be-assigned 10/751	
				Filing Date	December 8, 2003	
				First Named Inventor	Donald C. Stark et al.	
				Art Unit	2816	
				Examiner Name	Anh Quan Tra	
				Attorney Docket Number	9797-0147-999	

718

U.S. PATENT DOCUMENTS						
Examiner Initials	Document Number Number - Kind Code ¹	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Class	Subclass	Filing Date if Appropriate
<i>W</i>	5,194,765	03/16/1993	Dunlop et al.	326	87	06/28/91
<i>W</i>	5,254,883	10/19/1993	Horowitz et al.	326	30	04/22/92
	5,326,988	07/1994	Ishida, Ichiro	257	288	
	5,373,477	12/1994	Sugabayashi, Tadahiko	327	541	
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FOREIGN PATENT DOCUMENTS

Examiner Initials	Foreign Patent Document Country Code ² - Number ³ - Kind Code ⁴ (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Class	Subclass	Translation	
						Yes	No
<i>W</i>	EP 0 463 316 A1	01/02/1992		H04L	12/40		
<i>W</i>	EP 0 482 392 A2	04/29/1992		H04L	25/08		
<i>W</i>	JP 58-54412 (A)	03/31/1983		G05F1	56		

OTHER PRIOR ART - NON PATENT LITERATURE DOCUMENTS

Examiner Initials	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published					
<i>W</i>	Allen, Arnold O., "Probability, Statistics, and Queuing Theory with Computer Science Applications", 2nd Edition, CH 7, pp 450, 458-459					
<i>W</i>	Chappell, Terri I. et al., "A 2ns Cycle, 4ns Access 512 kb CMOS ECL SRAM", <i>IEEE International Solid State Circuits Conference</i> , 1991, pp 50-51					
<i>W</i>	Donnelly, Kevin S. et al., "A 660 MB\$ Interface Megacell Portable Circuit in 0.3 μm-0.7 μm CMOS ASIC", <i>IEEE Journal of Solid State Circuits</i> , 31(12):1995-2003 (1996)					
<i>W</i>	Pilo, Harold et al., "A 300 MHz 3.3V 1 Mb SRAM Fabricated in a 0.5 μm CMOS Process", <i>IEEE International Solid State Circuits Conference</i> , pp. 148-149 (1996)					
<i>W</i>	Schumacher, Hans-Jürgen et al., "CMOS Subnanosecond True-ECL Output Buffer", <i>IEEE Journal of Solid-State Circuits</i> , 25(1):150-154 (1990)					
<i>W</i>	Sidiropoulos, Stefanos et al., "A 700-Mb/s/bin CMOS Signaling Interface Using Current Integrating Receivers", <i>IEEE Journal of Solid-State Circuits</i> , 32(5):681-690 (1997)					
<i>W</i>	Yang, Tsen-Shau et al., "A 4-ns 4Kx1-bit Two-Port BiCMOS SRAM", <i>IEEE Journal of D-State Circuits</i> , 23(5):1030-1040 (1988)					

Examiner Signature	<i>W</i>	Date Considered	10/12/04
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INFORMATION DISCLOSURE CITATION  PTO-1449		<i>Complete If Known</i>	
		Application Number	10/731,718
		Filing Date	12/08/2003
		First Named Inventor	Donald C. Stark, et al.
		Art Unit	2816
		Examiner Name	Anh Quan Tra
		Attorney Docket Number	60809-0147-US
Sheet	1	of	1

U.S. PATENT DOCUMENTS

FOREIGN PATENT DOCUMENTS

Examiner Initials	Foreign Patent Document Country Code ³ - Number ³ - Kind Code ⁴ (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Class	Subclass	Translation	
						Yes	No
						X	

OTHER NON PATENT LITERATURE DOCUMENTS

Examiner Initials	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published
AS	EIA/JDEC, JC-42.3 Committee on RAM Memories, Minutes of Meeting 63, July 21, 1992, Denver, CO.
WT	EIA/JDEC, JC-42.3 Committee on RAM Memories, Minutes of Meeting 64, Sept. 16-17, 1992, Crystal City, VA.

**Examiner
Signature**



Date
Considered

10/12/02

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